DESCRIPTION

The MRF620R is a compact, fully integrated OOK/ASK receiver for 433.92 MHz frequency band. It requires few external components. The MRF620R consists of a low-noise amplifier (LNA), image-rejection mixer (IRM), built-in channel-select filter (CSF), OOK/ASK demodulator, data filter, and data slicing comparator. The local oscillator (LO) sub-system incorporates a monolithic VCO, ÷32 feedback divider, loop filter and fast start-up reference oscillator to form a complete phase-locked loop-based frequency synthesizer for single channel applications.

The MRF620R is available in an 8-pin SOP package and is specified over the temperature range from –20 to +70 °C.

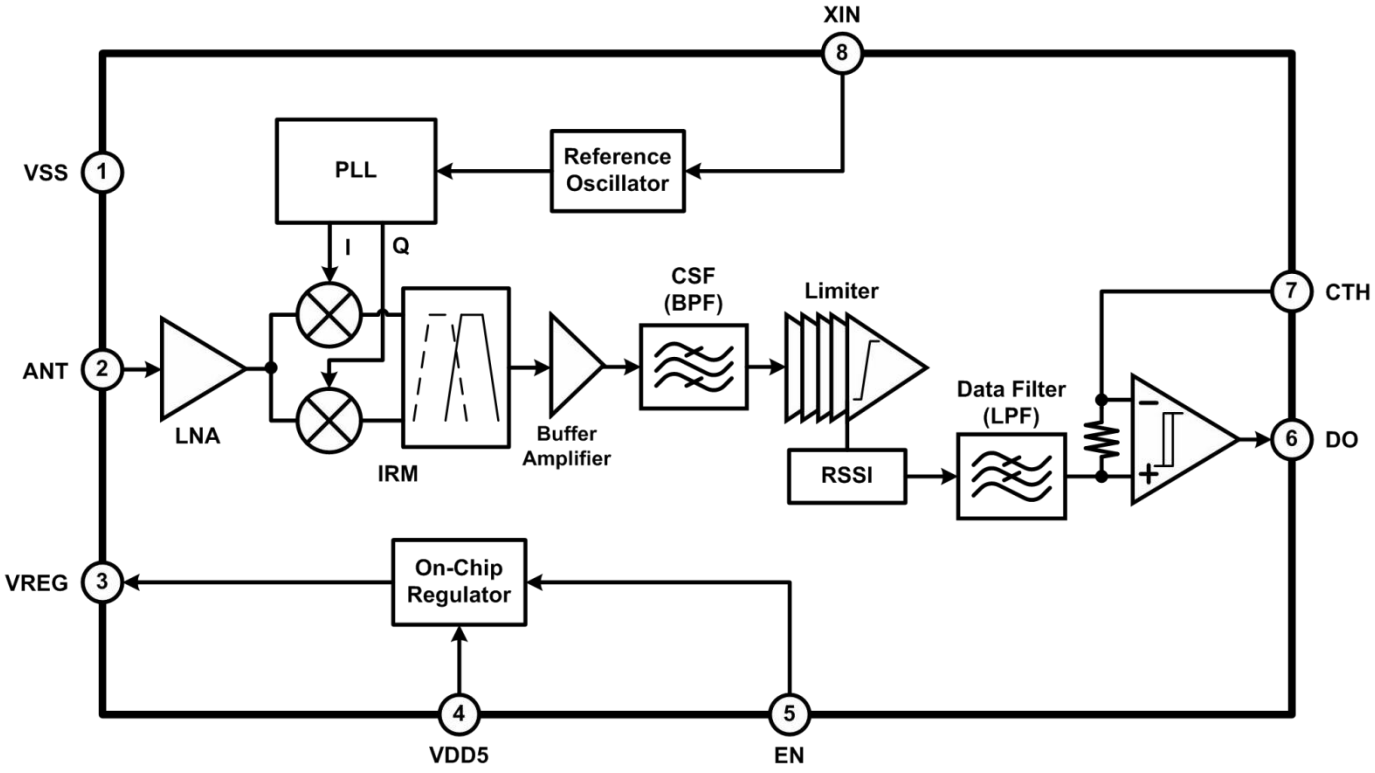
FEATURES

- Normal operating of 4.6 mA at 433.92 MHz
- Requires few external components
- Achieves sensitivity of –114 dBm (peak ASK signal level)
- Supply voltage range: 2.2 to 5.5 V
- Supports data rates up to 10 Kb/s
- Wide input dynamic range with automatic gain control handling
- Image-rejection ratio of 25 dB

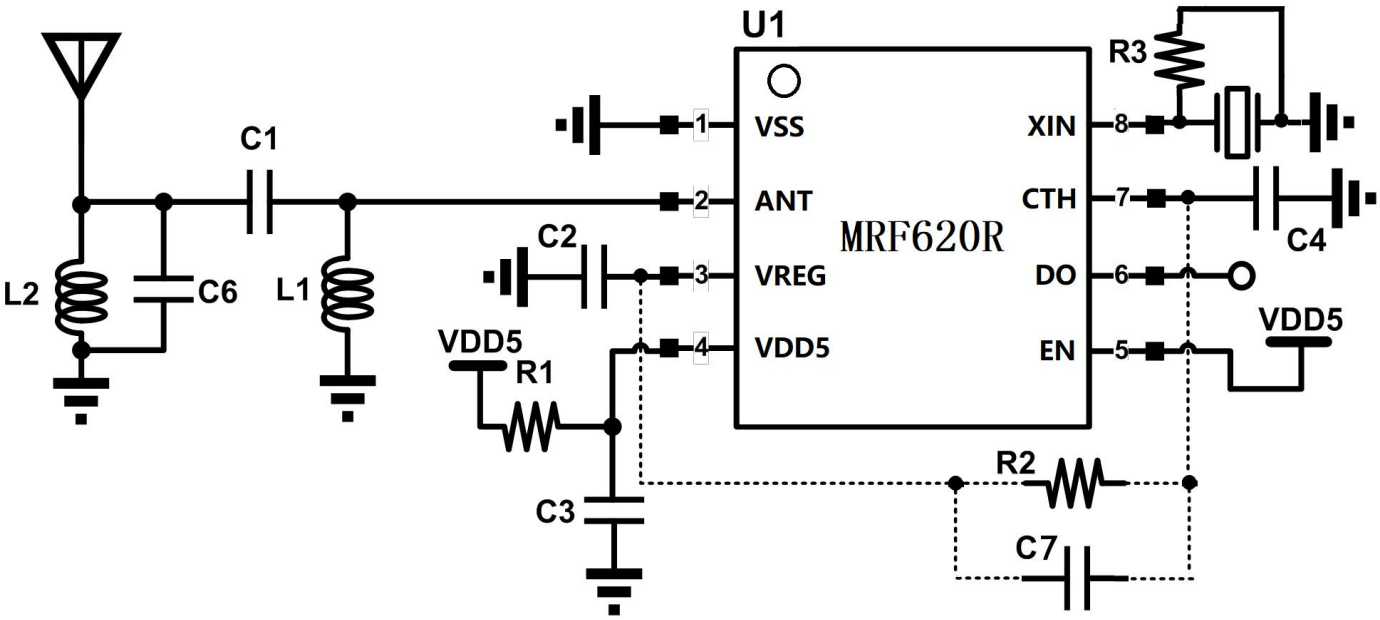
APPLICATIONS

- Automotive Remote Keyless Entry (RKE)
- Remote control
- Garage door and gate openers
- Suitable for applications that must adhere to either the European ETSI-300-220 or the North American FCC (Part 15) regulatory standards

BLOCK DIAGRAM



EVALUATION BOARD SCHEMATIC



BILL OF MATERIALS

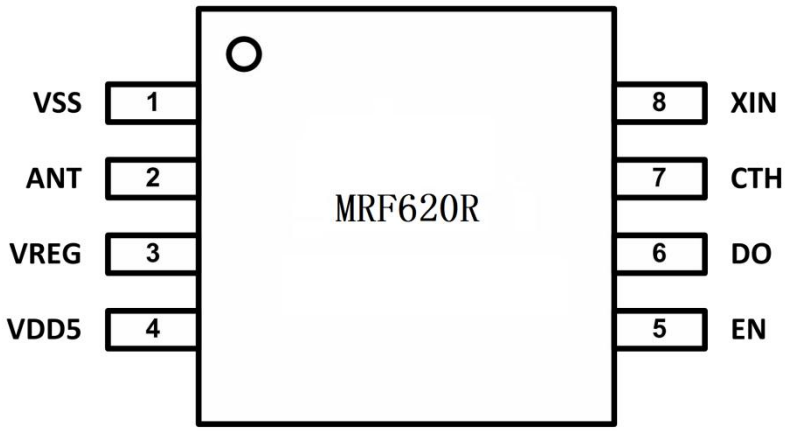
Part	Value	Unit	Description
L1	39 n	H	Antenna input matching
L2	22 n	H	Antenna input matching
C1	1.5 p	F	Antenna input matching
C2/C3	1u	F	Power supply de-coupling capacitor
C4	1u	F	C_{TH}, affects coding type and start-up time
C6	5.6p	F	Antenna input matching
C7	NC	F	Chip enable mode, C7 using 4.7uF capacitor will reduce the start-up time
R1	20	Ω	Power supply de-coupling resistor (optional)
R2	5.1M	Ω	For reducing data output noise (optional)
R3	2.2M	Ω	To set the bias point of the internal amplifier.
X1	13.598	MHz	Crystal with C_{Load} = *10 pF*, for reference oscillator
U1	MRF620R	U1	Receiver chip

Notes:
1. The value of C4 depends upon the data rate and coding pattern.
2. The *optional* components may be used depending upon specific application requirements.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
MRF620R	8 Pins, SOP, 150 mil	MRF620R

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	VSS	G	Ground
2	ANT	I	RF input connected to antenna via a matching network
3	VREG	P	Regulated core voltage
4	VDD5	P	5 V regulator input
5	EN	I	Chip enable (tie HIGH to enable the chip)
6	DO	O	Data output
7	CTH	I/O	Connection for data slicing threshold capacitor
8	XIN	I	Reference oscillator input

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD5}	–0.3	6	V
Analog I/O Voltage	—	–0.3	3	V
Digital I/O Voltage	—	–0.3	6	V
Operating Temperature Range	T_A	–20	+70	°C
Storage Temperature Range	T_{STG}	–40	+125	°C

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Conjunction Dissipation to External Environment	Rja	T_A = 27 °C	—	37.15	—	°C/W
From Chip Conjunction Dissipation to Package Surface	Rjc		—	1	1.8	

ELECTRICAL CHARACTERISTICS

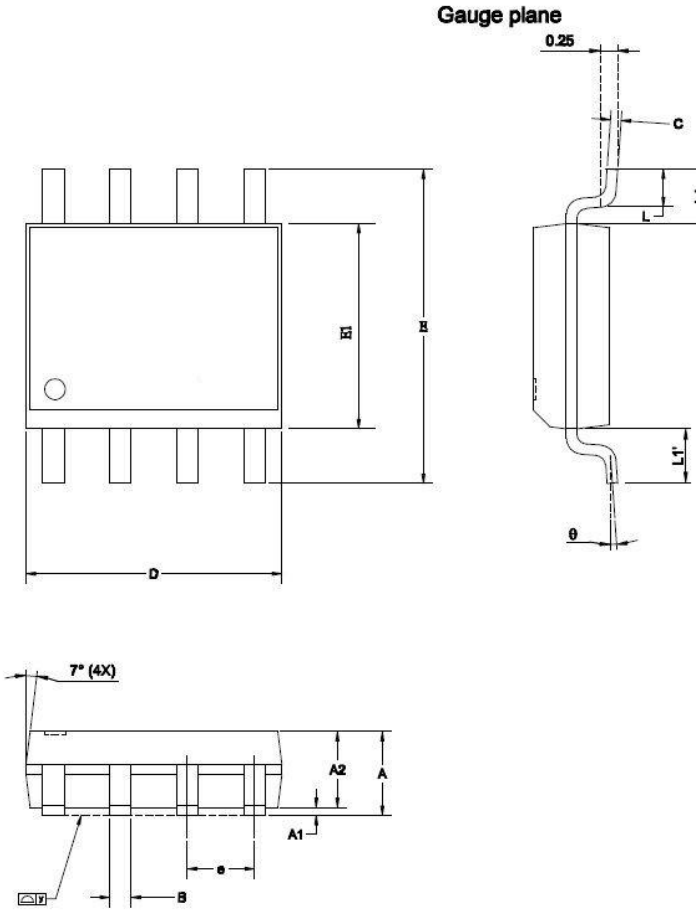
Nominal conditions: V_{DD5} = 5.0 V, V_{SS} = 0 V, f_{RF} = 433.92 MHz, CE = HIGH, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD5}	Supply voltage applied to VDD5 pin only	2.2	5.0	5.5	V
Current Consumption	I_{DD5}		—	4.6	—	mA
Standby Current	I_{STBY}	CE = LOW	—	—	1	µA
Operating Frequency Range	f_{RF}		410	—	450	MHz
Maximum Receiver Input Level	$P_{RF,MAX}$		–20	–15	—	dBm
Sensitivity[1]	S_{IN}	ASK[2], D_{RATE} = 2 Kb/s, Peak power level	—	–114	–	dBm
		OOK, D_{RATE} = 2 Kb/s, Peak power level	—	–114	–	
Data Rate	D_{RATE}		—	2	10	Kb/s
System Start-Up Time	T_{STUP}		—	—	—	ms
RF Front-End						
Image Rejection Ratio	IRR		—	25	—	dB
LO Leakage	L_{LO}	Measured at antenna input	—	—	–80	dBm
IF Section						
IF Center Frequency	f_{IF}		—	1.236	—	MHz
IF Bandwidth	BW_{IF}		—	380	—	KHz
RSSI Slope	SL_{RSSI}		—	11	—	mV/dB
Demodulator						
Post-Demodulator Filter Bandwidth	BW_{DF}		—	5.0	—	KHz
CTH Leakage Current	I_{ZCTH}	T_A = +85 °C	—	±100	—	nA
Phase-Locked Loop						
Reference Frequency	f_{REFOSC}		—	13.598	—	MHz
Reference Signal Voltage Swing[3]	V_{REF}	Peak-to-peak voltage (V_{PP})	0.3	—	2	V
Divider Ratio	DIV		—	32	—	—
Digital/Control Interface						
Input-High Voltage	V_{IH}	For CE pin	0.8 × V_{DD5}	—	—	V
Input-Low Voltage	V_{IL}	For AGCDIS, CE, FDIV, SELA and SELB pins	—	—	0.2 × V_{DD5}	V
Output Current	I_{OUT}	Source current at 0.8 × V_{DD5}	—	480	—	µA
		Sink current at 0.2 × V_{DD5}	—	600	—	
Output-High Voltage	V_{OH}	DO pin, I_{OUT} = –1 µA	0.9 × V_{DD5}	—	—	V
Output-Low Voltage	V_{OL}	DO pin, I_{OUT} = +1 µA	—	—	0.1 × V_{DD5}	V
Output Rise/Fall Times	t_R / t_F	DO pin, C_{LOAD} = 15 pF	—	2	—	µs

Notes:
1. Packet Error Rate (PER) < 1e-2 with one byte packet of $A5_{hex}$.
2. AM 99% with square-wave modulation
3. Depends on the ESR of crystal

PACKAGE INFORMATION

8 Pins, SOP (Small Outline Package with 3.9 mm ×4.9 mm Body Size, 1.27 mm Pitch Size and 1.5 mm Thick Body)



Symbol	Min.	Nom.	Max.
A	1.40	1.50	1.60
A1	0.00	—	0.10
A2	—	1.45	—
B	0.33	—	0.51
C	0.19	—	0.25
D	4.80	—	5.00
E1	3.80	3.90	4.00
e	—	1.27	—
E	5.80	6.00	6.20
L	0.40	—	1.27
y	—	—	0.1
θ	0°	—	8°
|L1－L1'|	—	—	0.12
L1	1.04 REF		

Notes:

1. Refer to JEDEC MS-012
2. Unit: mm